# **Design and Implementation of complex CMOS Logic gate**

**Objective:**

CMOS gate is a combination of two networks. It may find the output with using some different type of output. To use this microwind, we can easily get output and find the perfect value for the user.

**Theory:**

The expression may as:

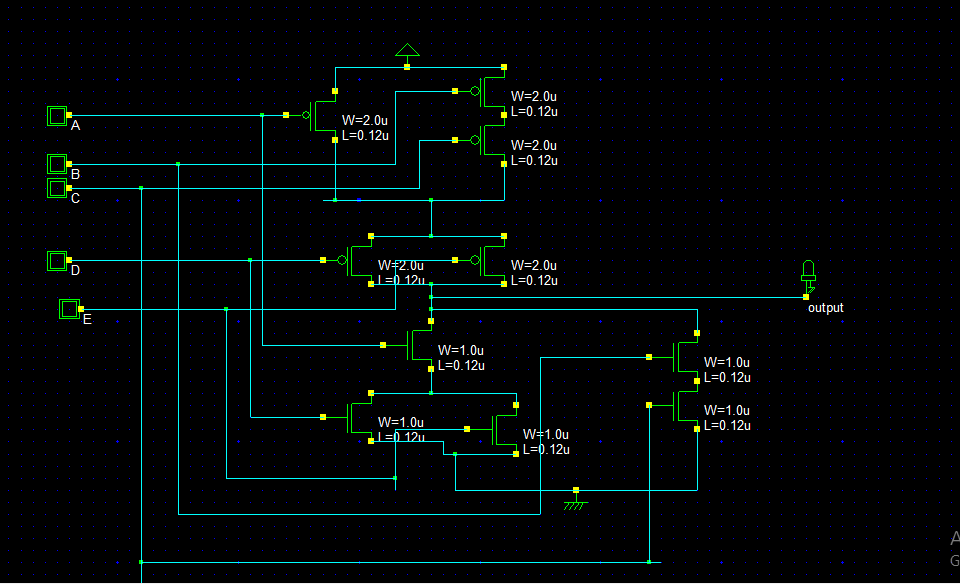
(A(D+E)+BC)’

Where, the input is A, B, C, D, and E and the output is only one value. That may find the value of on and off.

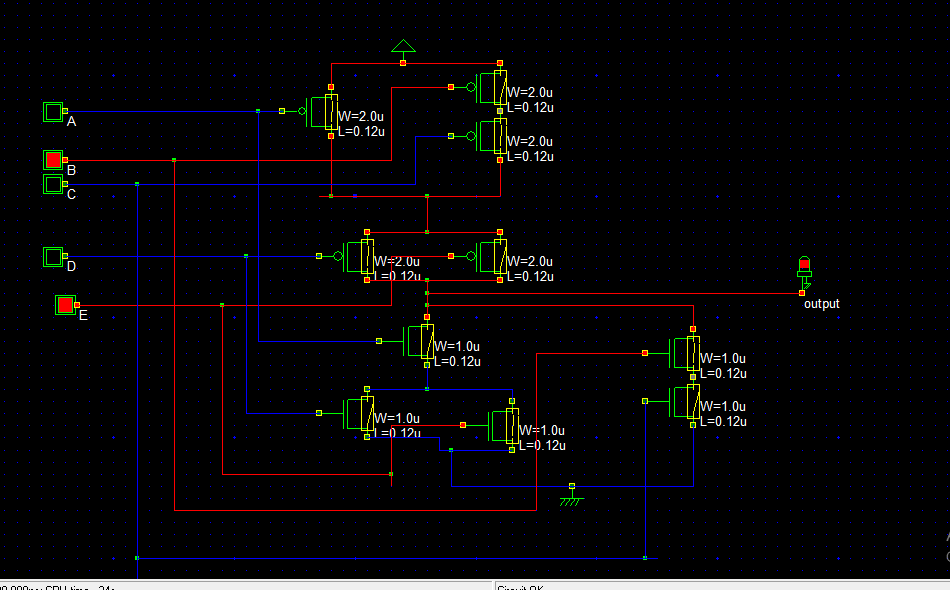
The Table can be written as:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | C | D | E | Y |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 |

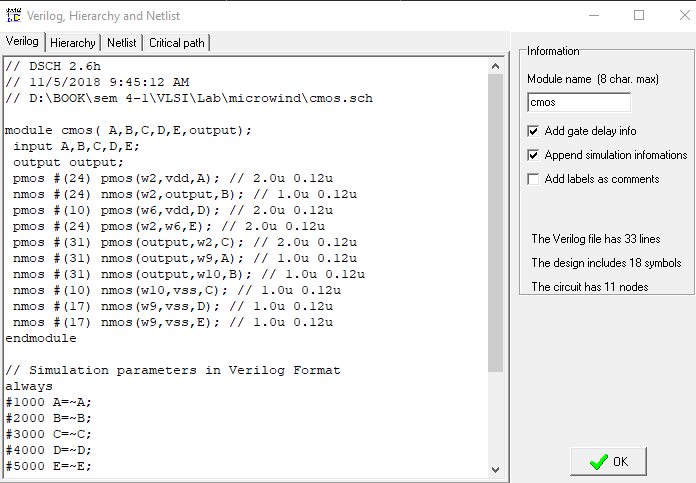
**Circuit Diagram** If all input is 0,other input 0 then output will be as



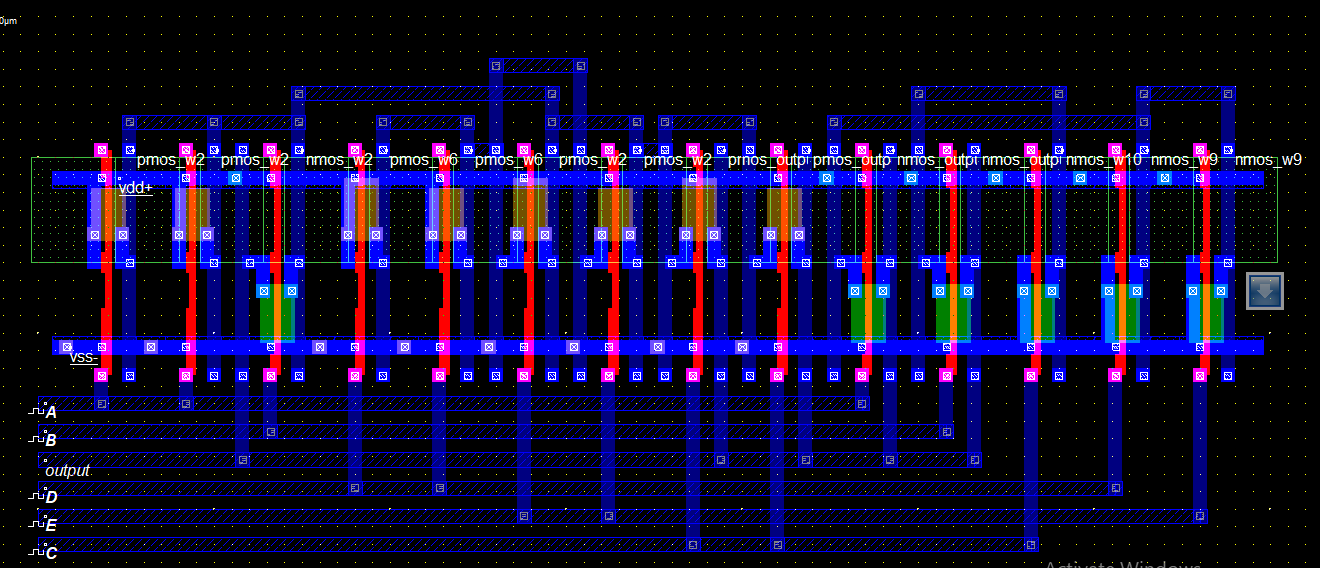
If two input same as 1, then output will be ON state.



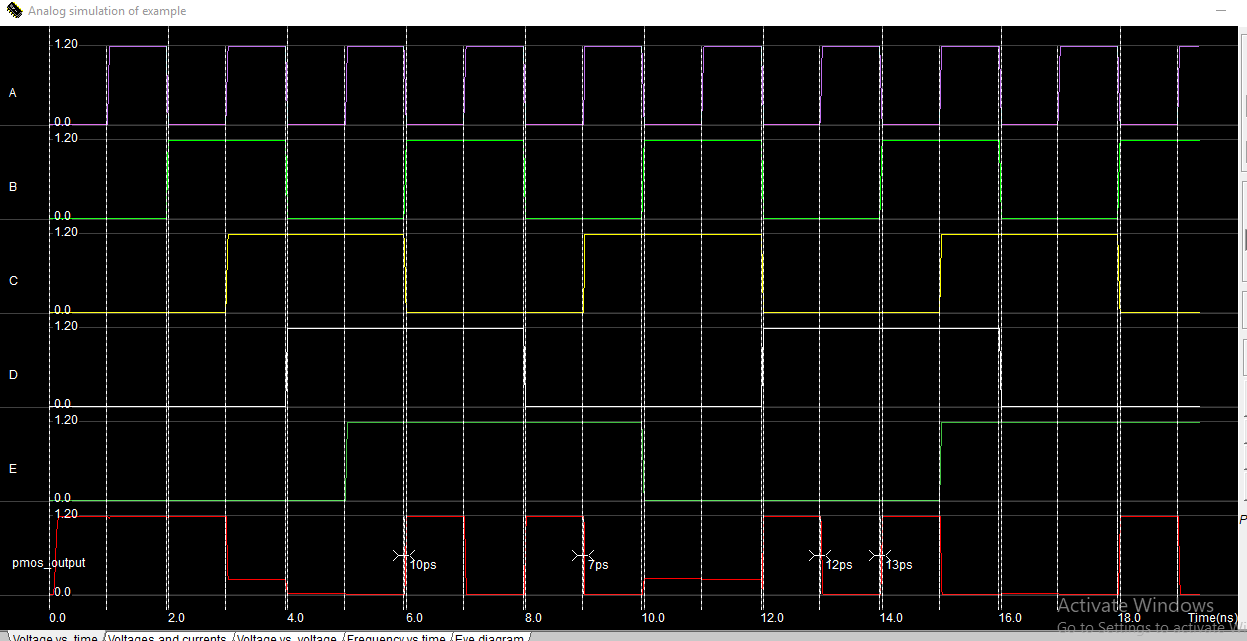
**Verilog File**



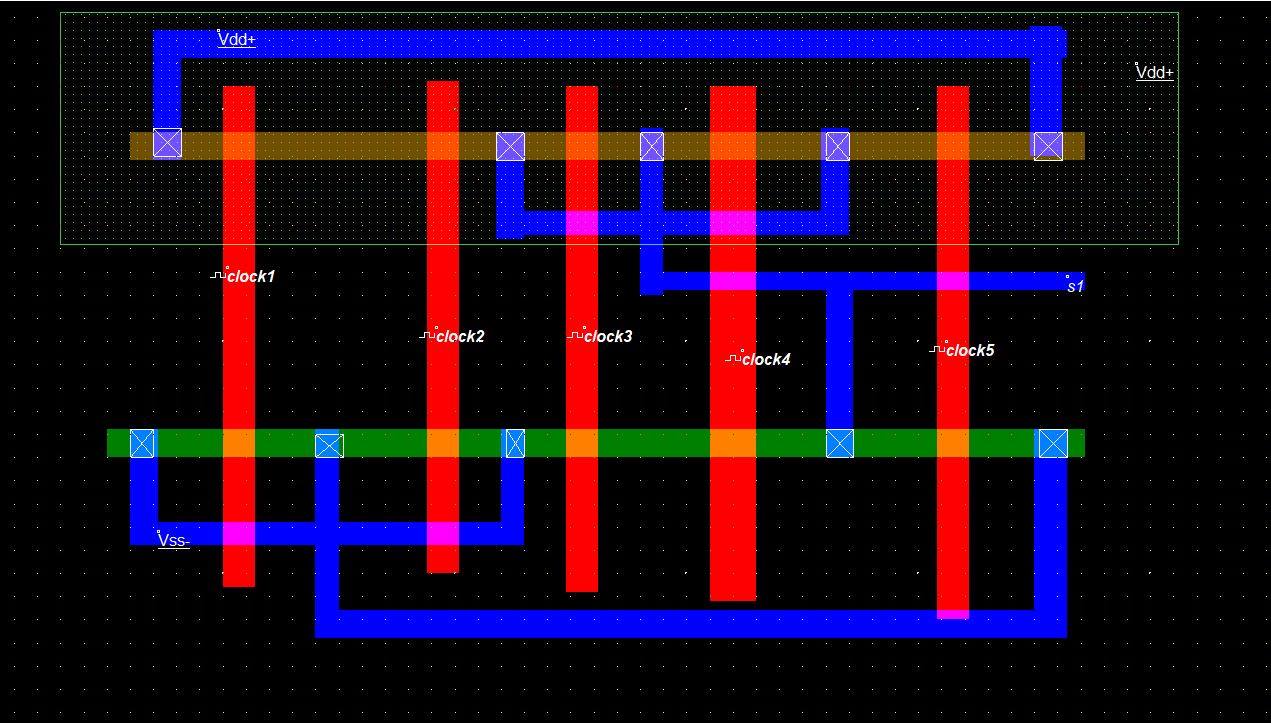
**Layout Diagram**

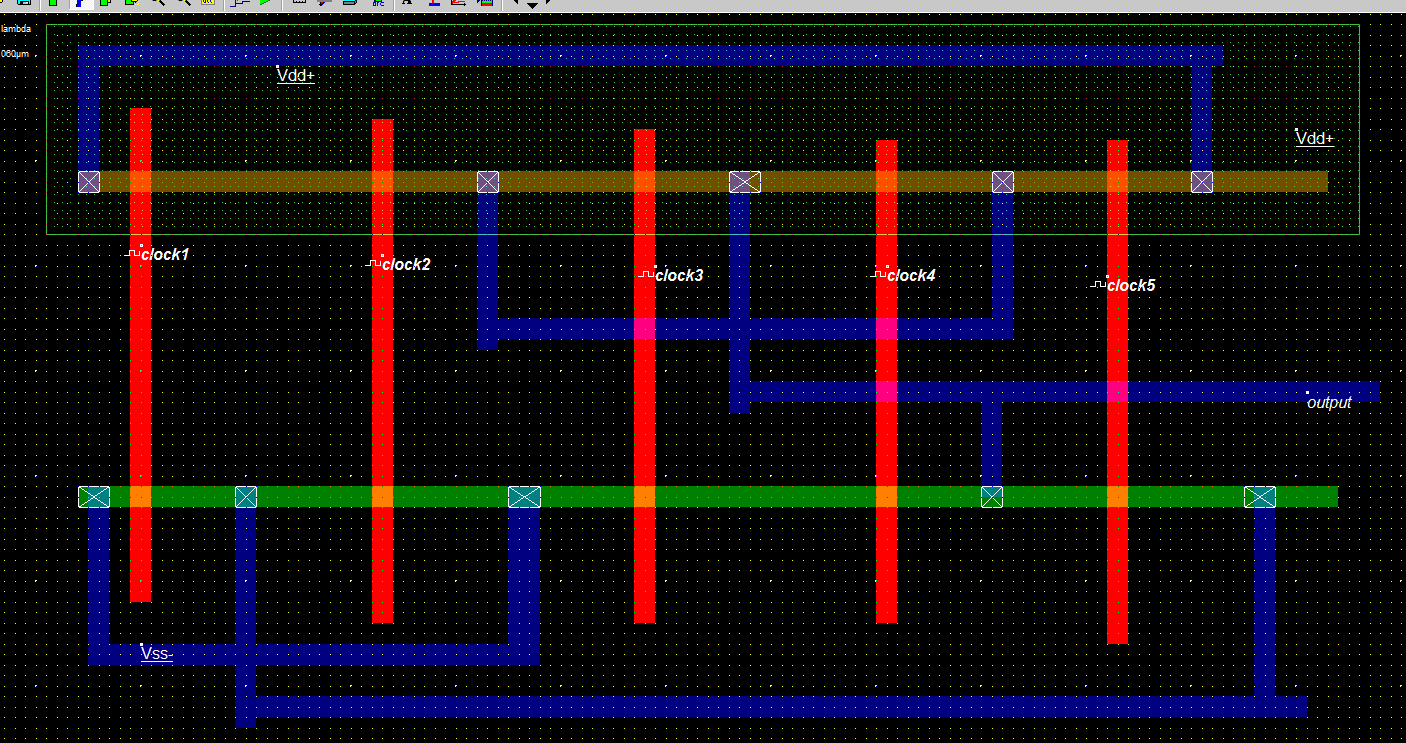
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**Timing Diagram**

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**Stick Diagram**

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**Timing Diagram**

**Discussion**

From this CMOS logic gate implementation, we can easily find the different type of expression. It can help us to find the different equation problem solving and find the output.